AMENDMENTS

In the Specification

On page 1, after the title and prior to the "Technical Field", please insert:

-- **RELATED PATENT DATA**

This patent resulted from a continuation application of U.S. Patent Application Serial No. 09/507,193 filed on February 18, 2000, now USPN 6,309,973 which is a continuation of U.S. Patent Application Serial No. 09/032,254, filed February 27, 1998. now USPN 6,083,803 --

In the Claims

Cancel Claims 1-11.

12. (Amended) A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface; and

unevenly removing material from the first uppermost surface of the conductive plug to define an uneven second uppermost surface at least a portion of which is disposed elevationally higher than the conductive lines and to reduce a width of the conductive plug from what it was prior to said unevenly removing.

2~~13~~. The m thod of claim 1~~2~~, wher in the un v nly removing material of the conductive plug comprises facet etching the conductive plug.

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Cancel Claims 14-15.

3~~16~~. (Amended) The method of claim 1~~2~~, wherein the forming of the conductive plug comprises forming the uneven uppermost surface of the plug to have a central region and a corner region joined therewith, and the unevenly removing material comprises removing more material from the corner region than from the central region of the first uppermost surface.

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Cancel Claims 17-20.

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~~21~~. (Amended) A method of increasing alignment tolerances between bit line contact material and storage capacitors in a DRAM comprising beveling at least one corner of a conductive plug formed over a diffusion region with which a bit line is to electrically communicate effectively to reduce a width of the conductive plug, the beveling changing a first generally even uppermost surface to a second generally uneven uppermost surface.

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22. (Amended) A method of forming DRAM circuitry comprising:

forming a conductive plug over a substrate node location between a pair of conductive lines and with which electrical communication with a bit line is desired, the conductive plug having a first uppermost surface having a generally uniform surface and having a width; and

etching material of the conductive plug to define a second uppermost surface which is generally non-planar and at least a portion of which is disposed elevationally higher than the conductive lines and to reduce the width of the conductive plug.

23. The method of claim 22, wherein the etching of the material of the conductive plug comprises facet etching the conductive plug.

Cancel Claims 24-46.

Add Claims 47-59

--47. (New) The method of claim 21 comprising beveling at least two corners of the conductive plug.

48. (New) A semiconductor processing method of forming integrated circuitry comprising:

forming a pair of spaced and adjacent conductive contact projections over a substrate, the conductive contact projections having respective widths and a generally even first uppermost surface;

etching at least one of the conductive contact projections effective to reduce its width, and form a generally uneven second uppermost surface;

forming insulative material over the conductive contact projections after the etching; and

etching at least one contact opening through the insulative material to at least one of the conductive contact projections proximate the other of the conductive contact projections.

49. (New) The method of claim 48 comprising etching both of the conductive contact projections to reduce their widths.

50. (New) The method of claim 48 wherein the etching comprises at least etching at least one outermost corner of the at least one conductive contact projection.

51. (New) The method of claim 12 wherein the unevenly removing comprises removing material of the conductive plug from an entirety of the uppermost surface.

52. (New) The method of claim 12 wherein the uppermost surface is substantially planar immediately prior to the unevenly removing.

53. (New) The method of claim 21 wherein the beveling is effective to reduce a height of the conductive plug over the diffusion region.

54. (New) The method of claim 22 wherein the etching etches material of the conductive plug from an entirety of the uppermost surface.

55. (New) The method of claim 22 wherein the uppermost surface is substantially planar immediately prior to the unevenly removing.

56. (New) The method of claim 48 wherein the one projection has an uppermost surface and the etching of the one projection etches material of the one projection from an entirety of the uppermost surface.

57. (New) The method of claim 48 wherein at least the one projection has an uppermost surface which is substantially planar immediately prior to the etching of the one projection.

58. (New) The method of claim 48 wherein the conductive projections have outermost surfaces which are entirely outwardly exposed during the etching of the at least one projection.

59. (New) A method of forming DRAM circuitry comprising:

forming a pair of spaced-apart, insulated conductive lines over a substrate, the conductive lines defining a node location therebetween;

forming insulative material over the node location and between the conductive lines;

forming an opening through the insulative material and between the lines to proximate the node location;

forming conductive material within the opening over the node location, the conductive material comprising an outer portion received elevationally outward of the insulated conductive lines, the conductive material having side surfaces which project away from the node location and terminate proximate an upper surface, the side surfaces and upper surface defining at least one corner region, the side surfaces defining a maximum width of the outer portion of the conductive material within the opening; and

beveling the at least one corner region effective to reduce the maximum width of the outer portion of the conductive material above the conductive lines and etching at least some of the conductive material away from an entirety of the upper surface.--